erage value. In contrast, the voltage-drop waveform appears as a sawtooth. Its mean rises as one-half of the duty cycle squared. The peak-voltage-drop value denotes a hypothetical voltage drop at the end of a whole period, T, of the SAMPLE/$\overline{\text{HOLD}}$ logic-control waveform.

You can use the previous **equations** to find the values of the voltage pedestal and the peak voltage drop. A 75% duty cycle is a convenient value. The following **equations** are valid for this duty cycle: $V_{INJ}=6[\Delta V_{OUT}]-2/3[\Delta V_{\overline{OUT}}]-16/3V_{STAT}$, and $V_{DROPPEAK}=16[-[\Delta V_{OUT}]+1/3[\Delta V_{\overline{OUT}}]+2/3V_{STAT}]$. You must find the optimal repetition rate, f_{REP}, of the logic-control signal. As the optimal repetition rate increases, the difference in output voltage from the input is almost purely due to dc voltage offset plus the voltage pedestal: $(V_{\overline{OUT}}-V_{STAT})/(V_{OUT}-V_{STAT})\simeq 3$. The following **equation** finds the maximum value for the optimal repetition rate: $f_{REP}\leq(0.01/4)\times 1/(t_{ON}-t_{OFF})$, where t_{ON} and t_{OFF} are the on and off times, respectively. This **equation** ensures that the difference in values between the turn-on and turn-off times of the sample-and-hold amplifier's internal analog switch won't affect the accuracy of the precision 25 and 75% duty cycles by more than 1%.

If you evaluate the **equation** for a high-performance analog switch, such as the Analog Devices (www.analog.com) ADG1213, you get a repetition rate of 33 kHz or less. The difference due to voltage drop prevails at low-value repetition rates. In this case, the repetition rate can be the value of the frequency at which $V_{\overline{OUT}}-V_{STAT}\leq 1/10\times V_{INMAX}$, where V_{INMAX} is the maximum input-voltage range. The best way to determine the lower limit of the repetition rate is through experimentation.

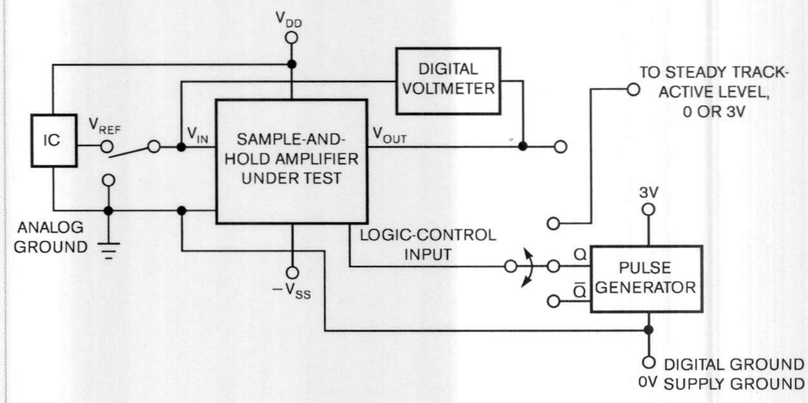

Figure 2 Use a digital voltmeter to measure the difference between the output and the input voltages of a sample-and-hold amplifier.

A tested sample-and-hold amplifier using the circuit in **Figure 2** uses a supply voltage of −1V, a drain-to-drain voltage of 5V, and a supply voltage of 3.3V for logic circuits in the pulse generator. Two sets of measurements at 25, 75, and 100% duty-cycle values for the AGD1213's internal switch control used input voltages of 0 and 2.5V. You will measure the output-voltage difference, approximately −0.0366 mV, and the pedestal voltage, approximately −0.0333 mV, at a repetition rate of 1.762 kHz. The value of the residual effective charge injection, Q_{INJ}, into the hold capacitor, $C_H=2$ nF, is $Q_{INJ}=C_H\times V_{INJ}$. The value is negative and doesn't exceed −75 fC. The following **equation** defines the difference of charge injection within the 2.5V range of input voltage: $\Delta Q_{INJ}=Q_{INJ}(2.5V)-Q_{INJ}(0V)$ and yields a value of −6.7 fC. The following **equation** determines the residual effective leakage current from the acquired values of peak voltage drop at a repetition rate of 160 Hz: $I_{LEAK}=C_H\times V_{DROPPEAK}\times f_{REP}$, where I_{LEAK} is the leakage current. A leakage current at the input voltage of 0V is approximately 17 pA, and a leakage current at the input voltage of 2.5V is approximately −17 pA. EDN

REFERENCE

1. "Low Capacitance, Low Charge Injection, ±15 V/+12 V iCMOSTM Quad SPST Switches," Analog Devices Inc, 2005, www.analog.com/en/switchesmultiplexers/analog-switches/adg1212/products/product.html.

Add hysteresis to a voltage comparator

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Positive feedback is a typical technique for distributing hysteresis around a comparator, provided that you have a resistive path between the comparator's output and the noninverting input. Positive feedback forms two threshold voltages that have (or assume) fixed values. In addition, they depend on the saturation values of the comparator's output stage. Plus, the load conditions affect their accuracy. The circuit in **Figure 1** provides an alternative for applications requiring a comparator with hysteresis that has precise thresholds that you can easily and independently set. The circuit includes two inverting and noninverting threshold comparators whose outputs directly drive a set/reset latch. You can use a latch with either active-low or active-high inputs.

You can generate the positive and negative threshold voltages using a

precision voltage reference that powers a resistor divider (not shown) or by driving the inputs with DACs if you need a digitally programmable comparator. The circuit's high input impedance facilitates this task. Because of its hold state, the latch nullifies the effects of frequent switching on the comparator's outputs due to noise on the input signal. The circuit thus acts as a Schmitt trigger even if there is no positive feedback. The latch introduces a propagation delay that's normally a few tens of nanoseconds and is negligible in low- to medium-speed applications. Because the latch has complementary outputs, the circuit provides a noninverting characteristic on the Q output and an inverting characteristic on the $\overline{Q}$ output (**Figure 1a** and **b**).

Some integrated latches have only the Q output. If you need an inverted output, you need only to exchange the comparator outputs with the latch inputs for both circuits; the upper comparator drives the reset input, and the lower comparator drives the set input. You can use open-collector or open-drain comparators to process bipolar or positive signals higher than the supply voltage of the latch. You can easily interface them without using clamping diodes. You must add only a pullup resistor that the logic supply powers.

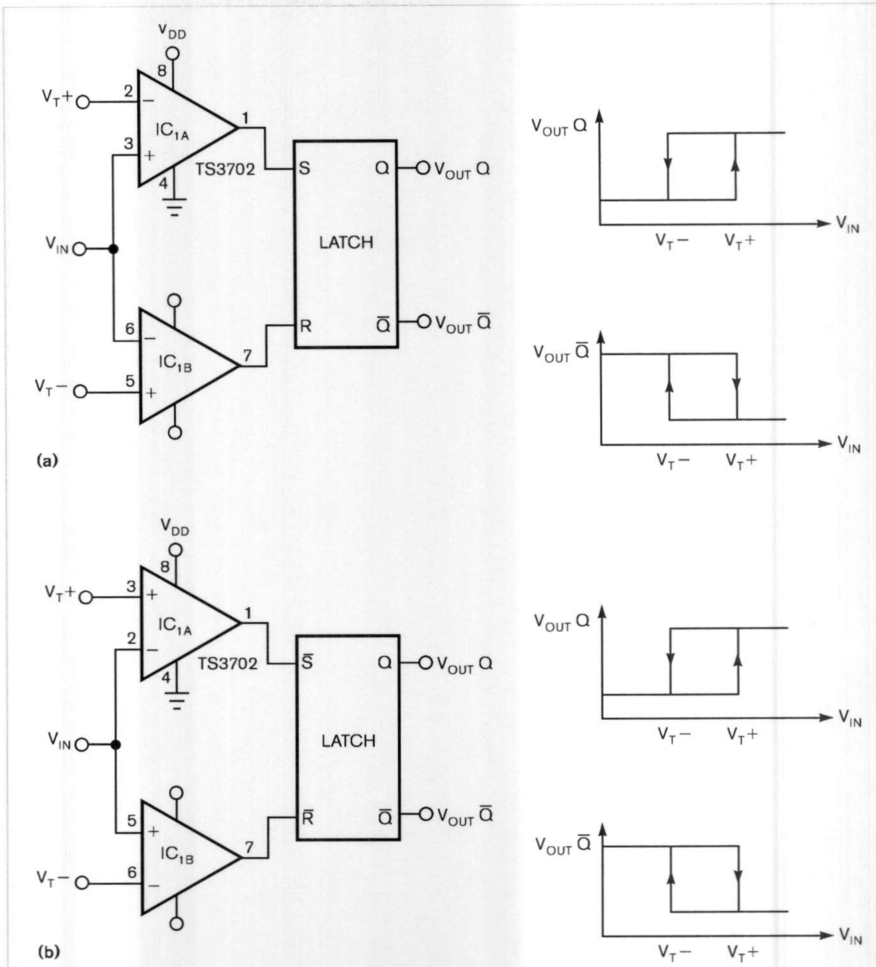

Figure 1 The set/reset latch provides hysteresis for the comparator. The circuit provides a noninverting characteristic on the Q output and an inverting characteristic on the $\overline{Q}$ output (a and b). Exchange the comparator outputs with the latch inputs for both circuits: The upper comparator drives the reset input, and the lower comparator drives the set input, and you get an inverting characteristic on the Q output and a noninverting characteristic on the $\overline{Q}$ output.

The circuit uses IC_1, an STMicroelectronics (www.st.com) dual micropower comparator with a push-pull output stage. In this case, the supply voltage must be the same as that for the latch. EDN

Broken-coil detector is simple yet robust

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The circuit in this Design Idea was originally designed to detect damaged conveyor belts in the mining industry. Thin coils are embedded in the conveyor belt. If the belt suffers damage, it stretches at the affected location, causing one or more coils to break. The method for detecting the broken coil is to allow a "sensing" coil to magnetically couple with the passing coils in the belt, thus changing the total inductance of the magnetic pair. The sensing coil is part of an LC oscillator (**Figure 1**). When an intact coil passes the sensing coil, the frequency of the oscillator changes. If the conveyor belt moves at a fixed speed, the frequency of the oscillator modulates